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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/814,568

03/31/2004

Vicki W. Tsai

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10/26/2005

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EXAMINER

WHITMORE, STACY

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/814,568

Applicant(s)

TSAI ET AL.

Examiner

Stacy A. Whitmore

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3-21, and 23-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Leaver (US Patent 6,195,788).

2. As for the following claims, Leaver discloses the invention as claimed:

1. A method comprising:

reading a design description for a heterogeneous reconfigurable device [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34];

combining functions within the design description into groups [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34 - mapping]; and

analyzing the groups for compliance with user-specified constraints [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34; col. 6, lines 59-62 - constraints].

3. The method of claim 1 wherein analyzing comprises estimating area occupied by the groups [col. 8, lines 58-64, determining cost or estimating];

4. The method of claim 1 further comprising re-combining functions into groups and re-analyzing the groups for compliance with the user-specified constraints [see as cited in the rejection of claim 1, and col. 12, lines 34-37, and 49-53 where the process is recursive and the logic reprogrammable];

5. The method of claim 1 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints [col. 8, lines 58-66];

6. The method of claim 1 further comprising compiling the functions to run on processing elements within the heterogeneous reconfigurable device [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34];
7. The method of claim 6 further comprising placement of the groups onto particular processing elements within the heterogeneous reconfigurable device [col. 3, lines 45-55; col. 4, lines 42-50];
8. The method of claim 7 further comprising analyzing the placement for compliance with user-specified constraints [col. 3, lines 45-67; col. 4, lines 42-50];
9. The method of claim 8 wherein analyzing the placement comprises estimating latency [col. 3, lines 62-64; col. 8, lines 58-64];
10. The method of claim 9 wherein estimating latency comprises estimating interconnect delay [col. 5, lines 55-58, col. 8, lines 58-64, the latency includes the delay of interconnects];
11. The method of claim 9 wherein estimating latency comprises estimating processing latency [col. 8, lines 58-64];
12. The method of claim 9 wherein estimating latency further comprises estimating processing latency and interconnect latency [col. 5, lines 55-58, col. 8, lines 58-64, the latency includes the delay of interconnects];
13. The method of claim 7 further comprising producing a file with a placed design for profiling [col. 8, lines 5-9, the Logic cone is a portion of a netlist that is used for profiling or a set of data showing significant features of the connectivity of elements];
14. The method of claim 13 further comprising profiling the design and comparing with user-specified constraints [col. 7, lines 26-43 show the logic cones being used to compare with user-specified constraints or criterion];
15. The method of claim 14 further comprising re-grouping functions in response to the profiling [col. 7, lines 25-42, especially lines 32-33 where the logic cones are used to do a final mapping];
16. The method of claim 14 further comprising re-performing placement in response to the profiling [col. 7, lines 25-42, especially lines 32-33 where the logic cones are used to do a placement or "fitted"];

17. A method comprising:

mapping a plurality of functions into groups [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34 - mapping];

placing the groups on resources within a heterogeneous reconfigurable device [col. 3, lines 45-55; col. 4, lines 42-50];

producing a mapped and placed design representation [col. 3, lines 45-64];

profiling the design representation [col. 7, lines 26-43 show the logic cones being used to compare with user-specified constraints or criterion]; and

comparing results from the profiling with user-specified constraints [col. 7, lines 26-43 show the logic cones being used to compare with user-specified constraints or criterion];

18. The method of claim 17 further comprising re-mapping the plurality of functions into groups [see as cited in the rejection of claim 1, and col. 12, lines 34-37, and 49-53 where the process is recursive and the logic reprogrammable];

19. The method of claim 17 further comprising re-placing the groups on resources [see as cited in the rejection of claim 1, and col. 12, lines 34-37, and 49-53 where the process is recursive and the logic reprogrammable];

20. The method of claim 17 wherein comparing results comprises comparing an estimated latency with a latency specified in the user-specified constraints [col. 8, lines 58-66];

21. The method of claim 20 wherein the estimated latency includes processing latency and interconnect latency [col. 5, lines 55-58, col. 8, lines 58-66, the latency includes the delay of interconnects];

23. An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine [col. 11, lines 18-48, especially element 706] performing:
reading a design description for a heterogeneous reconfigurable device [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34];

combining functions within the design description into groups [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34 - mapping]; and

analyzing the groups for compliance with user-specified constraints [abstract; col. 2, lines 32-37; col. 3, lines 47-64; col. 4, lines 28-34; col. 6, lines 59-62 - constraints];

24. The apparatus of claim 23 wherein the machine-accessible instructions when accessed further result in the machine performing:
re-combining functions into groups [see as cited in the rejection of claim 1, and col. 12, lines 34-37, and 49-53 where the process is recursive and the logic reprogrammable];
and
re-analyzing the groups for compliance with the user-specified constraints [see as cited in the rejection of claim 1, and col. 12, lines 34-37, and 49-53 where the process is recursive and the logic reprogrammable];
25. The apparatus of claim 23 wherein the machine-accessible instructions when accessed further result in the machine performing compiling the functions to run on processing elements within the heterogeneous reconfigurable device [see as cited in the rejection of claim 6];
26. The apparatus of claim 23 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints [see as cited in the rejection of claim 5];
27. An electronic system comprising: a processor; and a static random access memory to hold instructions that when accessed result in the processor performing reading a design description for a heterogeneous reconfigurable device, combining functions within the design description into groups, and analyzing the groups for compliance with user-specified constraints see as cited in the rejection of claim 1 and col. 11, lines 18-48, especially element 706 static RAM];
28. The electronic system of claim 27 wherein the instructions when accessed further result in the processor performing re-combining functions into groups, and re-analyzing the groups for compliance with the user-specified constraints [see as cited in the rejection of claim 4];
29. The electronic system of claim 28 wherein analyzing comprises comparing estimated parameters with prioritized user-specified constraints [see as cited in the rejection of claim 5].

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai (US Patent Application Publication 2005/0229139) or Honary (US Patent Application 2005/0193357).

The applied reference has a common assignee and/or inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

4. As for claims 1-29, Tsai or Honary disclose the invention as claimed, including the methods and system for reading a design, combining functions or mapping in a heterogeneous PLD, analyzing groups for compliance with user (prioritized) specified constraints, estimations of power, latency, timing, throughput, profiling, placement, re-

grouping, re-analyzing, SRAM [see Tsai; figs. 1-2, 6, pgs. 1-4, 6; see Honary; figs. 1, 3, 4, pgs. 1-4.]

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver (US Patent 6,195,788) in view of Jain (US Patent 6,038,386).

6. As for claims 2 and 22, Leaver discloses the invention substantially as claimed, including the methods of combining function "mapping " into groups and further comprising latency and throughput, as cited above in the rejection of claims 1, 12, and 17 above.

Leaver does not specifically disclose estimating power consumption.

Jain discloses estimating power consumption [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Leaver and Jain because adding the estimation

of power consumption to Leaver's method would have improved Leaver's method by minimizing power consumption and maintaining timing requirements of the PLD thereby improving the usage of programmable resources [see Jain, abstract].

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825



SAW
October 24, 2005